In configuration 0, the ACS unit associated with state 2n issues path metric PM(2n) to the next close pair. The two units of the pair receive the metric PM(n) of the preceding close pair. Path metric PM(2n+1) is issued to the common channel and path metric PM(n+N/2) is received from the common channel.

In configuration 1, the ACS units are swapped with respect to configuration 0, that is, the unit associated with state 2n+1 issues path metric PM(2n+1) to the next close pair. The only difference from configuration 0 is the external assigement of pads 50 through 54, which differentiates the way in which the pair of units is routed with the outside, as is shown for the connections with branch metrics BM00 and BM11.

In configuration 2, the unit associated with state 2n issues its path metric PM(2n) to the next close pair, and the two units receive path metric PM(n+N/2) from the preceding close pair. Path metric PM(2n+1) is issued to the common channel and path metric PM(n) is received from the common channel.

In configuration 3, the ACS units are swapped with respect to configuration 2, that is, the unit associated with state 2n+1 issues its path metric PM(2n+1) to the next close pair. The only difference from configuration 2 is the external assignment of pads 50 through 54.

The only topological difference between configurations 0 and 2 and between configurations 1 and 3 is the swapping of the connections to the pads 51 and 52 receiving the path metrics PM of a close pair and of a remote pair.

In these four configurations, connection crossings have been shown. Of course, these connections are implemented on two metallization layers.

Once the columns have been formed by juxtaposing the pairs, the connections which are not made by the juxtaposition are routed automatically, especially the connections of common channel 20 and the connections to the branch metric lines through the reduced local channels.

An advantage of the present invention is that some circuitry can be shared, without restraints, by the two units of each pair. This is in particular the case for a normalization circuit which is meant to control the overflow of path metric registers 10. This shared circuitry is located on the most significant bit side of the ACS units, that is, on the outer side of the circuit, the least significant bits being located on the side of central channel 20. This minimizes the connection length between two remote units, and thus increases the circuit speed.

In contrast, in the Sparso structure, a shared normalization circuit should be placed between the two units of a pair. The two units would then have symmetrical topologies, since the most significant bits should be on the side of the central normalization circuit. This symmetry would lead to an imbalance in length between the least significant lines on the side of the common channel and the least significant lines on the opposite side. This imbalance would lead to a decrease of the operating frequency.

FIG. 6 schematically illustrates an integrated structure obtained according to the invention of a network of ACS units in the example of a 64-state trellis. The number of the configuration used for each pair is indicated in a box 60 next to each pair, this box standing for the circuits shared between the two units of the pair.

Having thus described at least one illustrative embodiment of the present invention, various alterations, modifications, and improvements will readily occur to those skilled in the art. Such alterations, modifications, and improvements are intended to be within the spirit and the scope of the present invention. Accordingly, the foregoing description is by way of example only and is not intended as limiting. The present invention is limited only as defined in the following claims and the equivalents thereto.

What is claimed is:

1. An integrated structure for a network of N add-compare-select units associated with N states of a trellis of a Viterbi convolutive decoder, wherein within the integrated structure the N add-compare-select units are physically gathered by pairs of add-compare-select units juxtaposed to form two spaced apart parallel columns, each pair of add-compare-select units including two add-compare-select units associated, respectively, with states 2n and 2n+1 modulo-N where n is a positive integer, and each add-compare-select unit of the pair being coupled, for receiving two path metrics, to an add-compare-select unit associated with one of states n and n+N/2 of a close pair of add-compare-select units and to an add-compare-select unit associated with the other of states n and n+N/2 of a remote pair of add-compare-select units, a space between the two columns constituting a common channel including interconnections between remote pairs of add-compare-select units, wherein the integrated structure is implemented in a technology with at least three metallization layers and wherein the two add-compare-select units of each pair of add-compare-select units are physically juxtaposed withing the integrated structure along a column height of a respective column of the two columns.

2. The integrated structure of claim 1, wherein the N add-compare-select units have a same topology and each pair of add-compare-select units has a connection metallization topology adapted to one of four following configurations:

(A) the add-compare-select unit associated with state 2n is coupled to a next close pair of add-compare-select units and to the add-compare-select unit associated with state n of a preceding close pair of add-compare-select units;

(B) the add-compare-select unit associated with state 2n+1 is coupled to the next close pair of add-compare-select units and to the add-compare-select unit associated with state n of the preceding close pair of add-compare-select units;

(C) the add-compare-select unit associated with state 2n is coupled to the next close pair of add-compare-select units and to the add-compare-select unit associated with state n+N/2 of the preceding close pair of add-compare-select units; and

(D) the add-compare-select unit associated with state 2n+1 is coupled to the next close pair of add-compare-select units and to the add-compare-select unit associated with state n+N/2 of the preceding close pair of add-compare-select units.

3. The integrated structure of claim 2, wherein each add-compare-select unit of a respective pair of add-compare-select units is connected to two groups of branch metric supply lines out of four groups of branch metric supply lines, the four groups of branch metric supply lines being common to each add-compare-select unit in the respective column.

4. The integrated structure of claim 3, wherein each add-compare-select unit includes first, second, and third groups of pads for establishing connections with the next close pair of add-compare-select units and the add-compare-select units associated with states n and n+N/2, respectively.

and fourth and fifth groups of pads for establishing connections with the two groups of branch metric supply lines. respectively. all pads being arranged according to a topology common to all add-compare-select units.

5. The integrated structure of claim 4. wherein pads included in each group of pads are distributed along a width of the respective column. pads associated with most significant bits being located away from the common channel. where circuitry common to the two add-compare-select units of the respective pair of add-compare-select units is integrated.

6. The integrated structure of claim 1. wherein each add-compare-select unit of a respective pair of add-compare-select units is connected to two groups of branch metric supply lines out of four groups of branch metric supply lines. the four groups of branch metric supply lines being common to each add-compare-select unit in the respective column.

7. The integrated structure of claim 6. wherein each add-compare-select unit includes first. second. and third groups of pads for establishing connections with a next close pair of add-compare-select units and the add-compare-select units associated with states n and n+N/2. respectively. and fourth and fifth groups of pads for establishing connections with the two groups of branch metric supply lines. respectively. all pads being arranged according to a topology common to all add-compare-select units.

8. The integrated structure of claim 7. wherein pads included in each group of pads are distributed along a width of the respective column. pads associated with most significant bits being located away from the common channel. where circuitry common to the two add-compare-select units of the respective pair of add-compare-select units is integrated.

9. A Viterbi convolutive decoder comprising:

a network of N add-compare-select units. each of the N add-compare-select units being respectively associated with one state of an N state trellis of the Viterbi convolutive decoder. the N add-compare-select units being physically arranged within the Viterbi decoder to form two parallel columns. each of the two parallel columns including pairs of add-compare-select units that are physically arranged along a height of a respective column. each pair of add-compare-select units including first and second add-compare-select units that are associated with states 2n and 2n+1 modulo-N. respectively. where n is a positive integer. the first add-compare-select unit being coupled. for receiving a first path metric. to an add-compare-select unit that is associated with one of states n and n+N/2 of a close pair of add-compare-select units and the second add-compare-select unit being coupled. for receiving a second path metric. to an add-compare-select unit that is associated with the other of states n and n+N/2 of a remote pair of add-compare-select units; and

a common channel to separate the two parallel columns. the common channel including interconnections between remote pairs of add-compare-select units.

10. The Viterbi convolutive decoder of claim 9. wherein each add-compare-select unit of the N add-compare-select units is distributed throughout a width of the respective column.

11. The Viterbi convolutive decoder of claim 9. wherein connections between the first and second add-compare-select units of each pair of add-compare-select units are vertical.

12. The Viterbi convolutive decoder of claim 9. wherein the common channel includes only interconnections between remote pairs of add-compare-select units.

13. The Viterbi convolutive decoder of claim 9. wherein the Viterbi convolutive decoder is integrated in a structure that includes at least three metallization layers.

14. The Viterbi convolutive decoder of claim 9. wherein each of the N add-compare-select units have a same topology.

15. The Viterbi convolutive decoder of claim 14. wherein the first and second add-compare-select units of each pair of add-compare-select units includes connection metallization that couples the first and second add-compare-select units to other pairs of add-compare-select units in one of four configurations:

(A) the first add-compare-select unit is coupled to a next close pair of add-compare-select units and to the add-compare-select unit associated with state n of a preceding close pair of add-compare-select units;

(B) the second add-compare-select unit is coupled to the next close pair of add-compare-select units and to the add-compare-select unit associated with state n of the preceding close pair of add-compare-select units;

(C) the first add-compare-select unit is coupled to the next close pair of add-compare-select units and to the add-compare-select unit associated with state n+N/2 of the preceding close pair of add-compare-select units; and

(D) the second add-compare-select unit is coupled to the next close pair of add-compare-select units and to the add-compare-select unit associated with state n+N/2 of the preceding close pair of add-compare-select units.

16. The Viterbi convolutive decoder of claim 15. wherein the first and second add-compare-select units of each pair of add-compare-select units are connected to two groups of branch metric supply lines out of four groups of branch metric supply lines. the four groups of branch metric supply lines being common to each add-compare-select unit in the respective column.

17. The Viterbi convolutive decoder of claim 16. wherein the four groups of branch metric supply lines extend through a column height of the respective column and the two groups of branch metric supply lines that are connected to the first and second add-compare-select units of each pair of add-compare-select units are connected in reduced local routing channels.

18. The Viterbi convolutive decoder of claim 16. wherein the first and second add-compare-select units of each pair of add-compare-select units each includes:

a first group of pads connected to the next close pair of add-compare-select units;

a second group of pads connected to the add-compare-select unit associated with one of states n and n+N/2 of the preceding close pair of add-compare-select units:

a third group of pads connected to the add-compare-select unit associated with the other of states n and n+N/2 of the remote pair of add-compare-select units;

a fourth group of pads connected to a first group of branch metric supply lines of the two groups of branch metric supply lines; and

a fifth group of pads connected to a second group of branch metric supply lines of the two groups of branch metric supply lines.

19. The Viterbi convolutive decoder of claim 18. wherein pads included in each group of pads are distributed along a width of the respective column. pads associated with most significant bits being located away from the common channel.

20. The Viterbi convolutive decoder of claim 19. further comprising a normalization circuit coupled to each pair of add-compare-select units and located away from the common channel.

21. A Viterbi convolutive decoder comprising:

a network of N add-compare-select units implemented in a technology having at least three metallization layers, each of the N add-compare-select units being respectively associated with one state of an N state trellis of the Viterbi convolutive decoder, the N add-compare-select units being physically arranged within the Viterbi convolutive decoder to form two parallel columns, each respective parallel column of the two parallel columns including pairs of add-compare-select units physically arranged along a column height, each pair of add-compare-select units including first and second add-compare-select units that are associated with states 2n and 2n+1 modulo-N, respectively, where n is a positive integer, the first add-compare-select unit being coupled, for receiving a first path metric, to an add-compare-select unit that is associated with one of states n and n+N/2 of a close pair of add-compare-select units and the second add-compare-select unit being coupled, for receiving a second path metric, to an add-compare-select unit that is associated with the other of states n and n+N/2 of a remote pair of add-compare-select units;

a common channel to separate the two parallel columns, the common channel including interconnections between remote pairs of add-compare-select units; and

interconnection means, formed in the first and second add-compare-select units of each pair of add-compare-select units, for interconnecting the first and second add-compare-select units along a height of each respective parallel column to reduce a surface area of the network of N add-compare-select units.

22. The Viterbi convolutive decoder of claim 21, wherein the common channel includes only interconnections between remote pairs of add-compare-select units.

23. The Viterbi convolutive decoder of claim 21, wherein the interconnection means includes first connection metallization that couples the first and second add-compare-select units of each pair of add-compare-select units to other pairs of add-compare-select units in one of four configurations:

(A) the first add-compare-select unit is coupled to a next close pair of add-compare-select units and to the add-compare-select unit associated with state n of a preceding close pair of add-compare-select units;

(B) the second add-compare-select unit is coupled to the next close pair of add-compare-select units and to the add-compare-select unit associated with state n of the preceding close pair of add-compare-select units;

(C) the first add-compare-select unit is coupled to the next close pair of add-compare-select units and to the add-compare-select unit associated with state n+N/2 of the preceding close pair of add-compare-select units; and

(D) the second add-compare-select unit is coupled to the next close pair of add-compare-select units and to the add-compare-select unit associated with state n+N/2 of the preceding close pair of add-compare-select units.

24. The Viterbi convolutive decoder of claim 23, further comprising four groups of branch metric supply lines extending along the height of each of the respective parallel columns and in common with both the respective parallel columns, wherein the interconnection means further includes second connection metallization that connects the first and second add-compare-select units of each pair of add-compare-select units in the respective parallel column to two groups of branch metric supply lines of the four groups of branch metric supply lines.

25. The Viterbi convolutive decoder of claim 24, wherein:

the first connection metallization includes a first group of pads connected to the next close pair of add-compare-select units, a second group of pads connected to the add-compare-select unit associated with one of states n and n+N/2 of the preceding close pair of add-compare-select units, and a third group of pads connected to the add-compare-select unit associated with the other of states n and n+N/2 of the remote pair of add-compare-select units; and

the second connection metallization includes a fourth group of pads connected to a first group of branch metric supply lines of the two groups of branch metric supply lines, and a fifth group of pads connected to a second group of branch metric supply lines of the two groups of branch metric supply lines.

26. The Viterbi convolutive decoder of claim 25, wherein pads included in each group of pads are distributed along a width of the respective column, pads associated with most significant bits being located away from the common channel.

27. The Viterbi convolutive decoder of claim 26, further comprising a normalization circuit coupled to each pair of add-compare-select units and located away from the common channel.

28. The Viterbi convolutive decoder of claim 21, further comprising four groups of branch metric supply lines extending along the height of each of the respective parallel columns and in common with both the respective parallel columns, wherein the interconnection means includes connection metallization that connects the first and second add-compare-select units of each pair of add-compare-select units in the respective parallel column to two groups of branch metric supply lines of the four groups of branch metric supply lines.

29. An integrated structure for a network of N add-compare-select units associated with N states of a trellis of a Viterbi convolutive decoder, wherein within the integrated structure the N add-compare-select units are physically gathered by pairs of add-compare-select units juxtaposed to form two spaced apart parallel columns, each pair of add-compare-select units including two add-compare-select units associated, respectively, with states 2n and 2n+1 modulo-N where n is a positive integer, and each add-compare-select unit of the pair being coupled, for receiving two path metrics, to an add-compare-select unit associated with one of states n and n+N/2 of a close pair of add-compare-select units and to an add-compare-select unit associated with the other of states n and n+N/2 of a remote pair of add-compare-select units, wherein the integrated structure is implemented in a technology with at least three metallization layers and wherein the two add-compare-select units of each pair of add-compare-select units are physically juxtaposed withing the integrated structure along a column height of a respective column of the two columns.